

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE



In re Application of:

Andreas et al.

Serial No.: 10/645,710

Filed: August 21, 2003

For: WAFER CLEANING METHOD AND
RESULTING WAFER

Confirmation No.: 8457

Examiner: Tu Tu V. Ho

Group Art Unit: 2818

Attorney Docket No.: 2269-5663US
(02-1325.00/US)

Notice of Allowance Mailed:

January 26, 2005

CERTIFICATE OF MAILING

I hereby certify that this correspondence along with any attachments referred to or identified as being attached or enclosed is being deposited with the United States Postal Service as First Class Mail on the date of deposit shown below with sufficient postage and in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

February 25, 2005
Date

Signature

Leah J. Barrow
Name (Type/Print)

TRANSMITTAL LETTER

Mail Stop Issue Fee
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

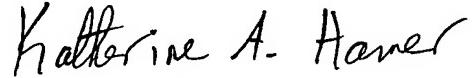
Sir:

Applicants submit herewith Part B - Fee(s) Transmittal for the above-captioned application and a check in the amount of \$1715.00 in payment therefor plus five (5) copies of the patent when issued.

Applicants understand that no additional fees are required. However, if the Office determines that any comparison fees or other additional fees are required, the Commissioner is

authorized to charge any such fees to TraskBritt Deposit Account No. 20-1469. A copy of this Transmittal Letter is enclosed for deposit account charging purposes.

Respectfully submitted,



Katherine A. Hamer
Registration No. 47,628
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Date: February 25, 2005

KAH/djp:ljb

Enclosures: Part B - Issue Fee Transmittal

Check No. 21395 in the amount of \$1715.00

Copy of Transmittal Letter

Amendment under 37 C.F.R. § 1.312

Fee Addressee for Receipt of PTO Notices Related to Maintenance Fees

Document in ProLaw



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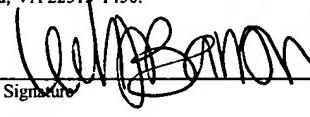
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COMMENTS ON STATEMENT OF REASONS FOR ALLOWANCE

Mail Stop Issue Fee
Commissioner for Patents
PO Box 1450
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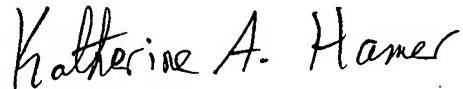
Sir:

The Examiner indicates:

The prior art of record fails to teach or render obvious a method of cleaning a semiconductor wafer including at least one registration mark having all exclusive limitations as recited in claims 1, 19, and 30, comprising providing a semiconductor wafer comprising at least one registration mark and exposing the semiconductor wafer to a cleaning solution, the at least one registration mark comprising at least one trench having a trench width from approximately 1.0 μm to approximately 3.0 μm , the cleaning solution either comprising tetramethylammonium hydroxide and at least one surfactant, the at least one surfactant as recited in claims 1 and 19, or the cleaning solution consisting essentially of tetramethylammonium hydroxide and at least one surfactant, the at least one surfactant comprising at least one acetylenic diol surfactant.

Applicants concur with the reasons as stated by the Examiner insofar as they comprise a summary, and are exemplary and not limiting. In addition, the allowed dependent claims include other and further features and elements than those specified by the Examiner. Accordingly, the scope of the claims must be determined from the literal language of each as a whole, as well as equivalents thereof.

Respectfully submitted,



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